	Title	Current OR	Current XRef
10	Mechanism for screening commands issued over a communications bus for selective execution by a processor	713/200	340/825.52; 710/240
11	Networked facilities management system having a node configured with distributed load management software to manipulate loads controlled by other nodes	713/324	713/300
12	Method and apparatus for the secure communication of data	379/357.04	235/380; 379/257; 379/354; 379/361; 379/418; 379/444; 379/93.28; 713/184
13	Advanced massively parallel computer using a field of the instruction to selectively enable the profiling counter to increase its value in response to the system clock	712/16	712/245
14	Low power architecture for portable and mobile two-way radios	455/575	455/343; 455/574; 455/90; 712/32
15	Multipurpose bus interface utilizing a digital signal processor	712/40	703/25; 712/37
16	Method and apparatus for controlling initiation of bootstrap loading of an operating system in a computer system having first and second discrete computing zones	713/2	
17	Multiple processing cell digital data processor	712/16	712/18
18	Central processing apparatus for generating and receiving time division multiplex signals	713/400	

	Title	Current OR	Current XRef
1	Fault isolation for communication networks for isolating the source of faults comprising attacks, failures, and other network propagating errors	713/201	709/224; 714/57
2	Programmable microcontroller architecture for disk drive system	712/244	710/266; 711/171; 711/219; 712/227
3	Network server platform for a hybrid fiber twisted pair local loop network service architecture	370/404	370/906; 713/201
4	Bidirectional communication port for digital signal processor	712/35	370/439; 709/235; 709/237; 712/34
5	Advanced massively parallel computer with a secondary storage device coupled through a secondary storage interface	712/11	711/114; 711/119; 712/13; 712/20
6	Information storage device for storing personal identification information	379/357.03	235/380; 379/355.08; 379/357.04; 379/361; 379/93.02; 379/93.03; 713/184; 713/186
7	Human factored interface incorporating adaptive pattern recognition based controller apparatus	713/600	348/110; 348/27; 348/734; 712/240; 712/245
8	Fraud detection and user validation system for mobile earth terminal communication device	380/247	340/5.61; 340/5.8; 380/270; 713/171
9	Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal	709/400	713/400; 713/500

	Title	Current OR	Current XRef
60	Multi-phase multi-access pipeline memory system in which the pipeline memory can decode addresses issued by one processor while simultaneously accessing memory array by other processor	713/500	711/100; 713/501
61	Power saving control by predetermined frequency slot timing signal based start index and halt instruction termination signal	713/320	713/323; 713/501
62	Secure storage device for transfer of digital camera data	713/192	
63	Switching method in a multi-threaded processor	709/107	709/108; 712/219; 712/228; 712/229
64	Data processor	712/241	712/205; 712/207
65	Data manipulation instruction for enhancing value and efficiency of complex arithmetic	708/490	708/495; 712/221
66	VLIW processor for exchanging and inputting sub-instructions to containers, and code compression device and method for compressing program code	712/24	711/125; 712/212; 712/228
67	Computer system including a device with a plurality of identifiers	710/104	710/10; 713/1
68	Digital timing recovery using baud rate sampling	713/400	360/51; 713/600
69	Virtual shadow registers and virtual register windows	712/244	710/260

	Title	Current OR	Current XRef
46	Devices, systems and methods for mode driven stops	714/30	712/227
47	Method and apparatus for low power, micro-electronic mechanical sensing and processing	340/870.05	340/870.01; 340/870.11; 340/870.16; 713/324
48	Digital signal processor and power control circuit	713/322	713/323
49	Speaker verification interface for secure transactions	713/186	705/75
50	Authentication system, and contents-information sender and receiver	713/156	
51	Optimization methods for the insertion, protection, and detection of digital watermarks in digital data	713/176	
52	Secure computing device including virtual memory table look-aside buffer with non-relocatable page of memory	713/200	
53	Contents-information transmission system	713/201	
54	Method and apparatus for contents information	705/51	380/277; 380/284; 713/193
55	Efficient handling of a large register file for context switching and function calls and returns	712/228	
56	Method and apparatus for contents information	705/51	380/278; 713/193
57	Data processor	712/210	
58	Processor executing unpack instruction to interleave data elements from two packed data	712/225	712/22; 712/223; 712/300
59	Signal recording apparatus, signal record medium and signal reproducing apparatus	380/201	380/277; 380/287; 713/189; 713/193; 713/200

	Title	Current OR	Current XRef
31	Data processing apparatus with register file bypass	712/218	
32	N-dimensional biometric security system	713/202	
33	Systems and methods for detecting tampering of a computer system by calculating a boot signature	713/200	713/2
34	Embedded-DRAM-DSP architecture	712/228	712/32
35	Programmable logic integrated circuit devices including dedicated processor components	326/38	712/226
36	Embedded-DRAM-DSP architecture	712/228	712/32
37	High-throughput asynchronous dynamic pipelines	712/216	
38	MMU descriptor having big/little endian bit to control the transfer data between devices	711/201	711/130; 711/203; 712/204
39	Multistandard video decoder and decompression system for processing encoded bit streams including pipeline processing and methods relating thereto	712/300	
40	Digital signal processor particularly suited for decoding digital audio	712/42	708/209; 708/490; 708/497; 712/220; 712/32; 712/36
41	Accessing diagnostic program counter value data within data processing systems	712/11	
42	Embedded-DRAM-DSP architecture	712/228	
43	Single instruction multiple data processing	712/221	712/223
44	System and method for utilizing programmed multi-speed operation with a microprocessor to reduce power consumption	713/322	
45	Electronic apparatus and processing ability alteration instruction apparatus	713/330	

	Title	Current OR	Current XRef
17	System and method for authorization of access to a resource	713/185	
18	Method and apparatus for instruction set architecture to perform primary and shadow digital signal processing sub-instructions simultaneously	712/35	712/36
19	Parallel data communication having skew intolerant data groups	713/503	713/400
20	System and method for communicating a secure unidirectional response message	713/170	
21	Data recording apparatus, data recording method, and data transfer system	380/227	713/168
22	Data processing circuits and interfaces	712/221	712/245
23	Clock system for multiple component system	713/500	
24	Multistandard video decoder and decompression system for processing encoded bit streams including storing data and methods relating thereto	712/300	
25	Multiprocessor system. multiprocessor control method, and multiprocessor control program retaining computer-readable recording medium	712/35	712/39
26	Battery management system employing software controls upon power failure to estimate battery duration based on battery/equipment profiles and real-time battery usage	713/300	
27	Security access method and apparatus	713/202	340/5.82; 382/115
28	Data processor	712/244	712/241
29	Security animation for display on portable electronic device	713/200	
30	Shuffle instructions	712/223	

	Title	Current OR	Current XRef
1	Apparatus and systems for dyadic digital signal processing instructions	712/35	712/209; 712/221
2	Instruction set architecture for signal processors	712/35	712/209; 712/221
3	Multistandard video decoder and decompression system for processing encoded bit streams including expanding run length codes and methods relating thereto	712/300	375/253
4	Dyadic DSP instructions for digital signal processors	712/35	
5	Methods of dyadic DSP instruction operation	712/35	
6	Receiver with automatic skew compensation	713/503	
7	Watermark systems for media	386/46	348/473; 348/474; 386/95; 713/176
8	Hardware architecture, operating system and network transport neutral system, method and computer program product for secure communications and messaging	713/201	713/151; 713/176
9	Collusion-resistant watermarking and fingerprinting	713/176	380/44
10	Background watermark processing	713/176	380/205
11	Automation of signal processing apparatus	700/94	713/400
12	System and method for secure unidirectional messaging	713/153	
13	System and method for conducting a secure response communication session	709/227	709/237; 713/200
14	Transaction verification system and method	705/75	713/168
15	Apparatus and method for bus power measurement in a digital signal processor	713/300	
16	System and method for conducting a secure interactive communication session	713/201	713/150